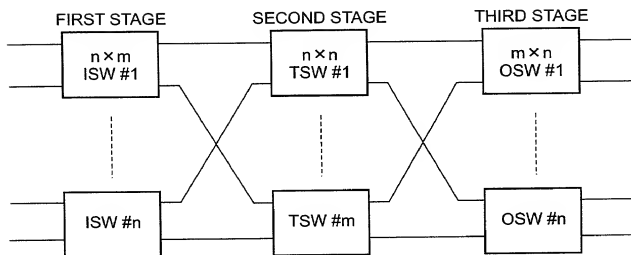


FIG.1 PRIOR ART



09376904.001299

FIG. 2 PRIOR ART

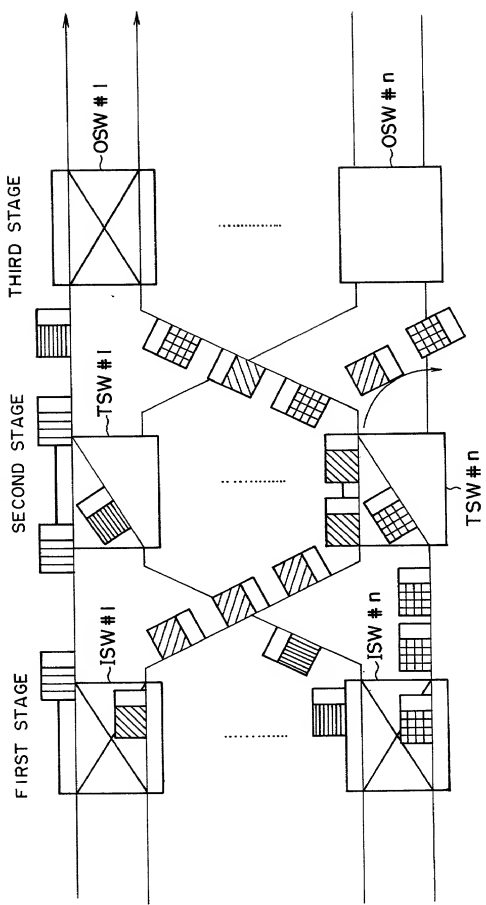


FIG. 3 PRIOR ART

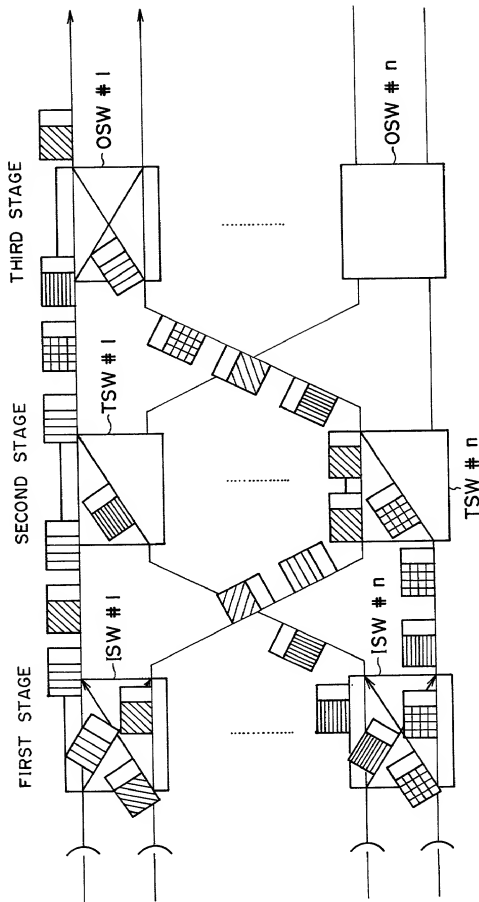


FIG.4 PRIOR ART

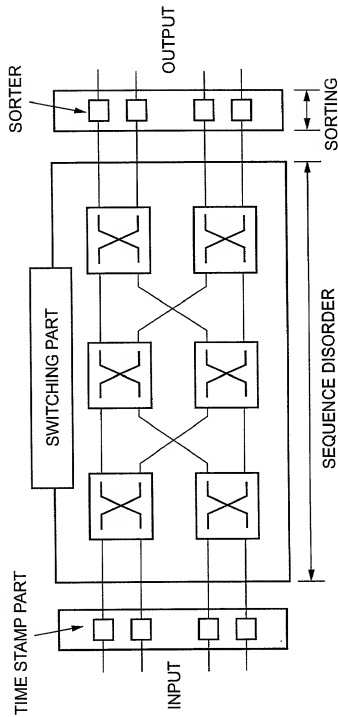


FIG. 5 PRIOR ART

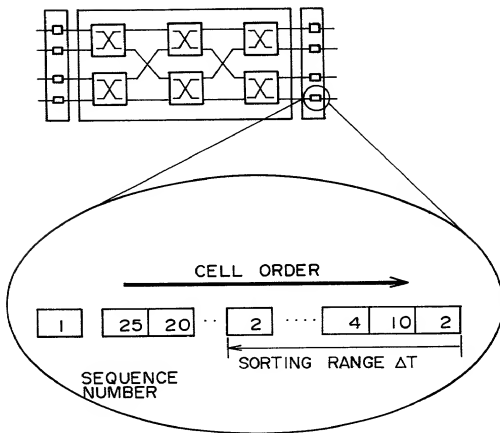


FIG. 6 PRIOR ART

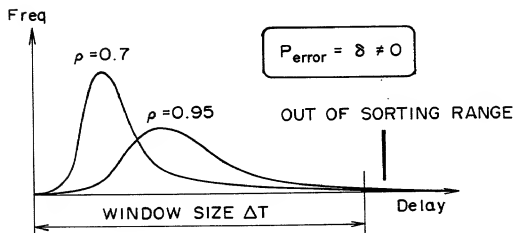


FIG.7 PRIOR ART

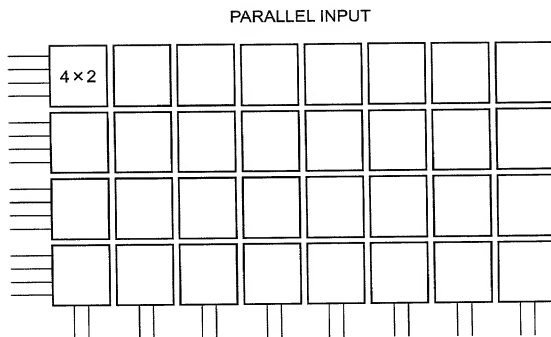


FIG.8 PRIOR ART

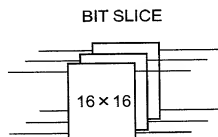


FIG.9 PRIOR ART

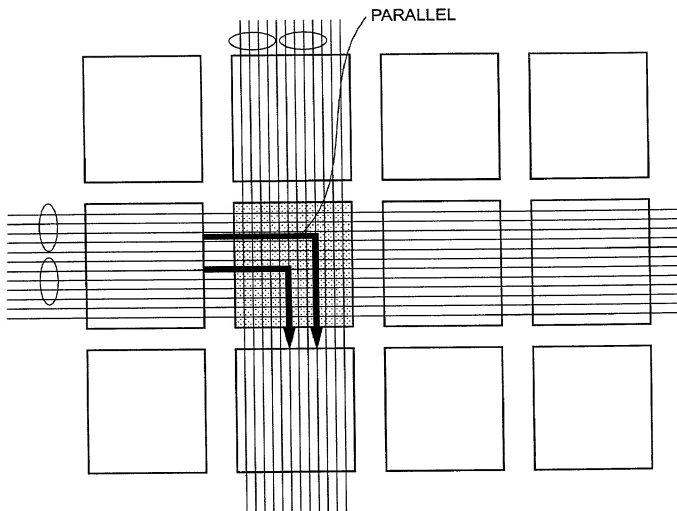


FIG.10 PRIOR ART

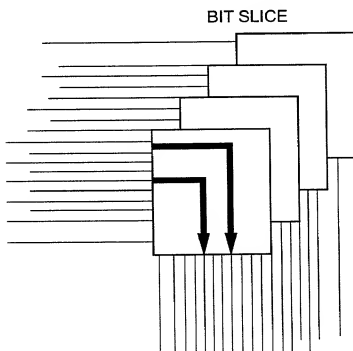


FIG. 11

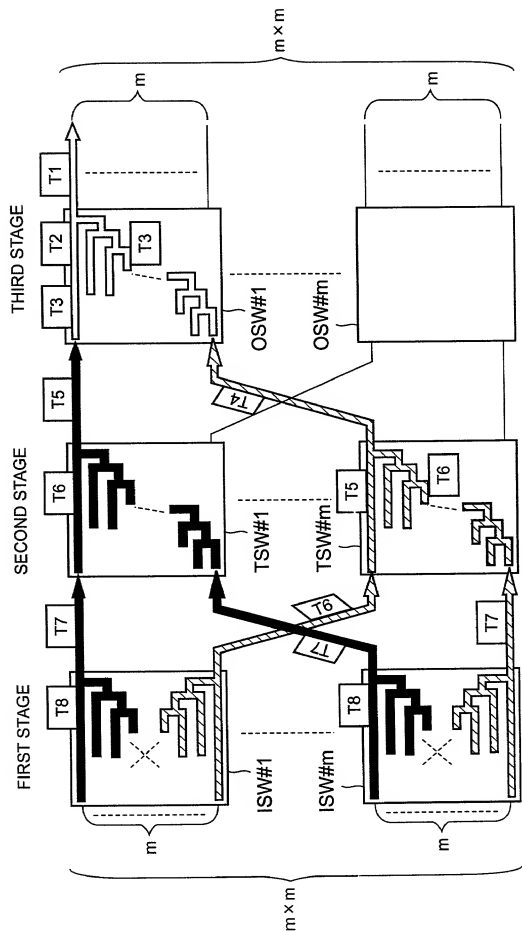




FIG.12

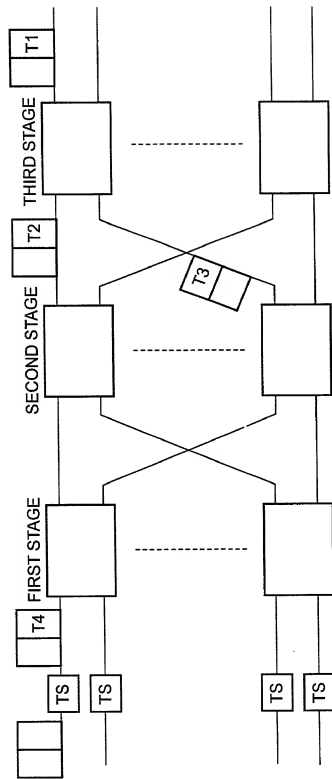
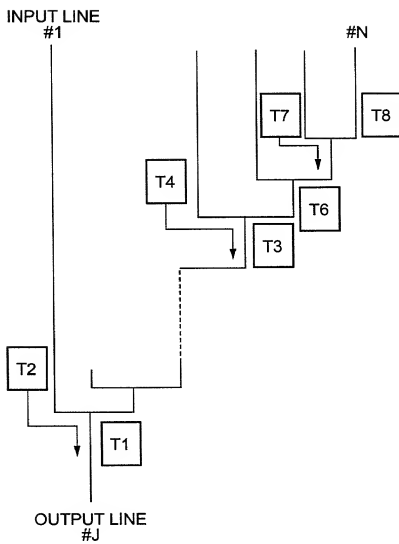
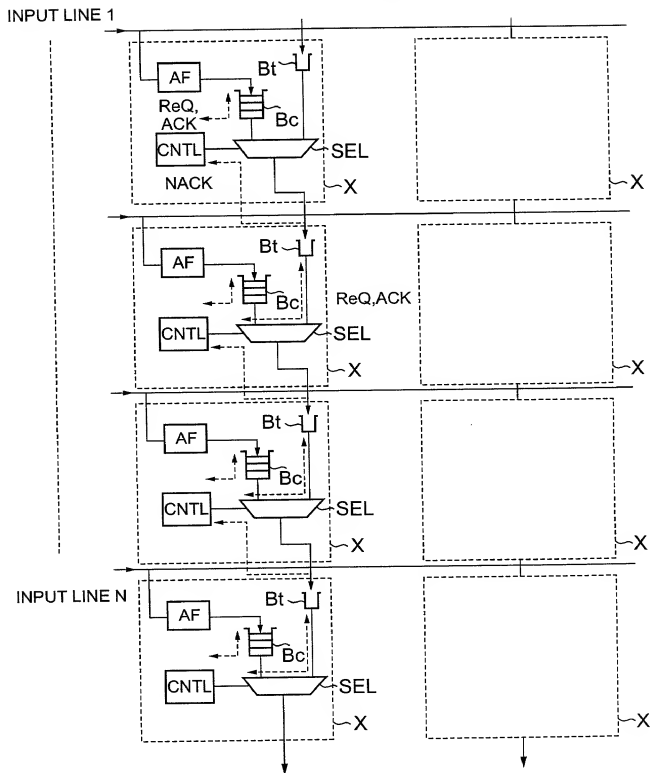


FIG.13



09376904.081899

# FIG.14



00375904.001899

FIG.15

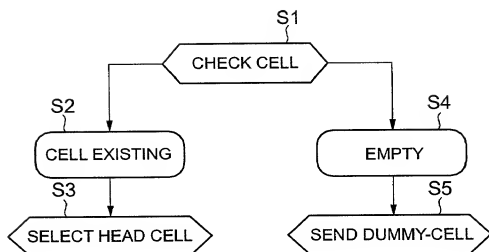


FIG. 16

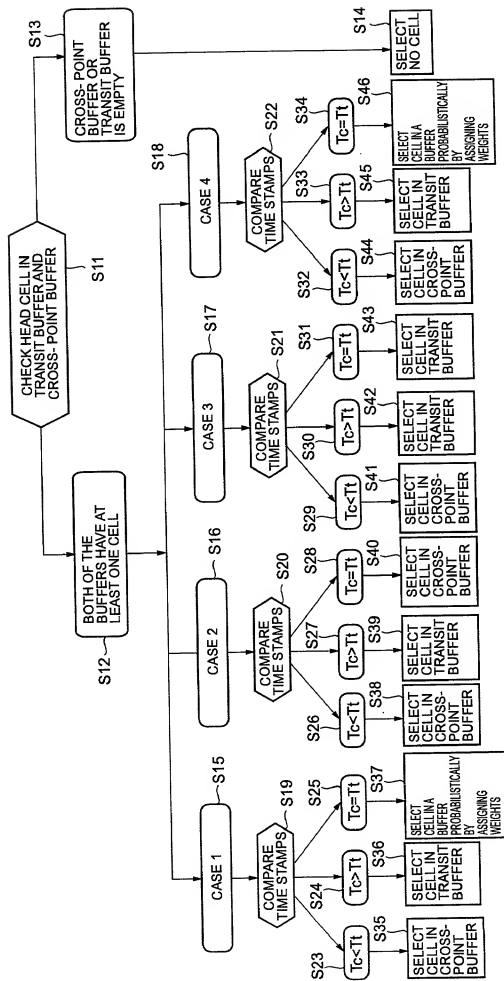


FIG.17

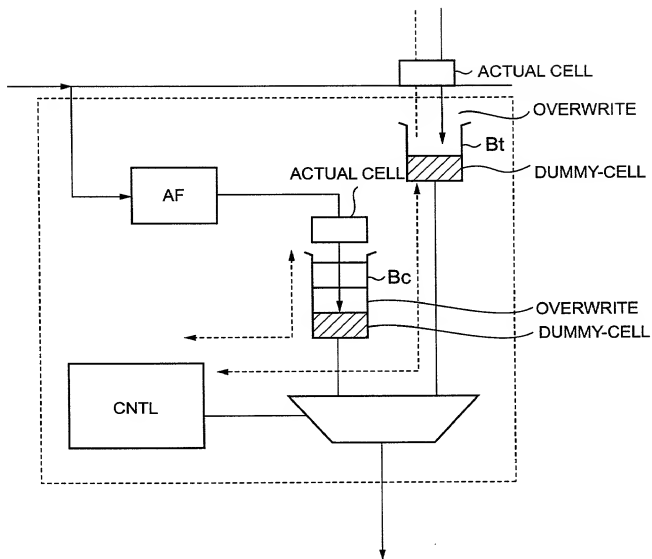


FIG.18

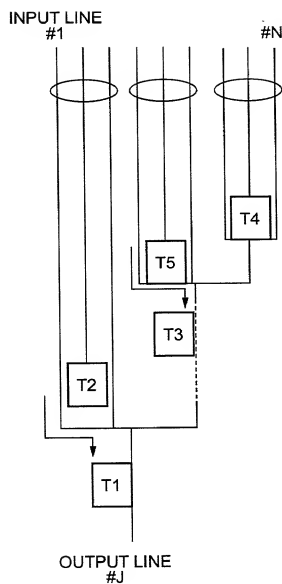


FIG.19

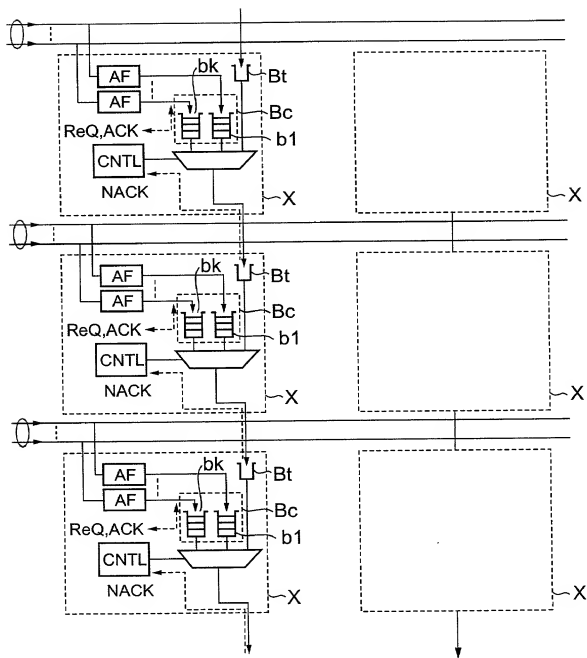
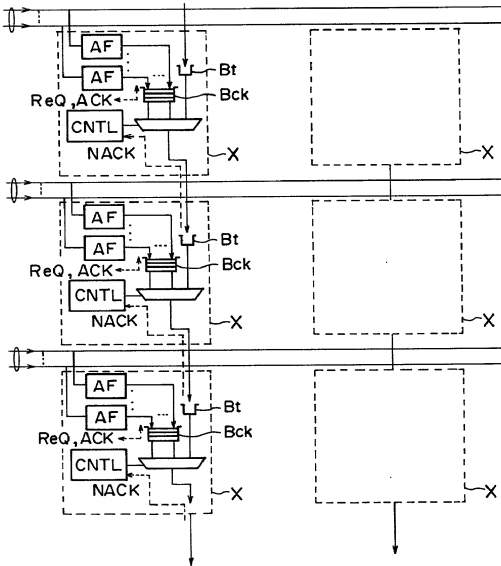


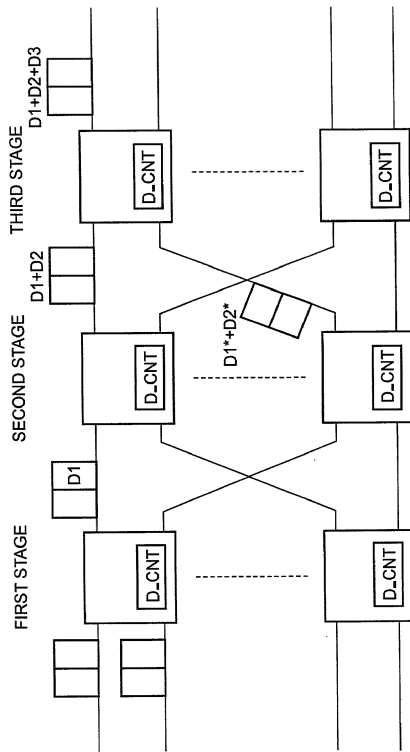


FIG. 20



09376904.001899

FIG.21



# FIG. 22

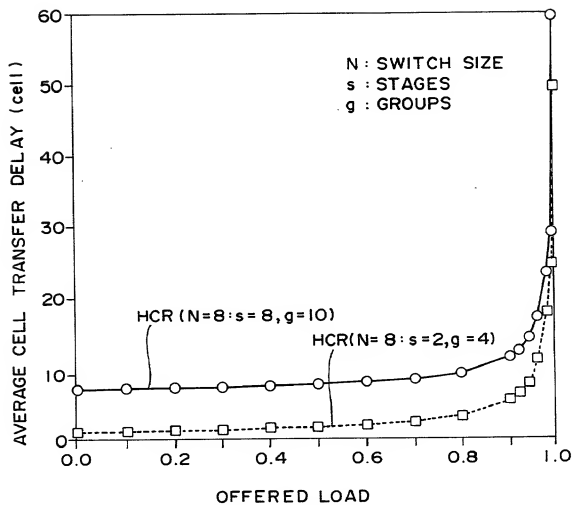


FIG.23

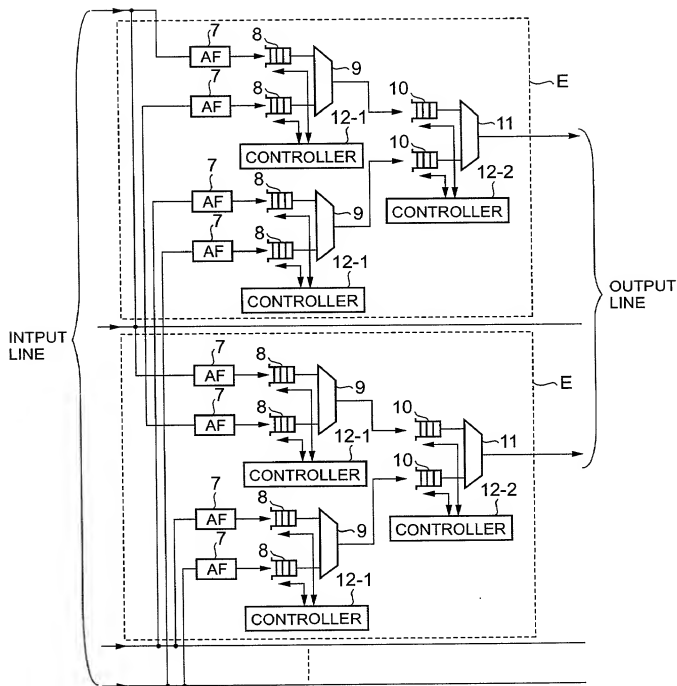
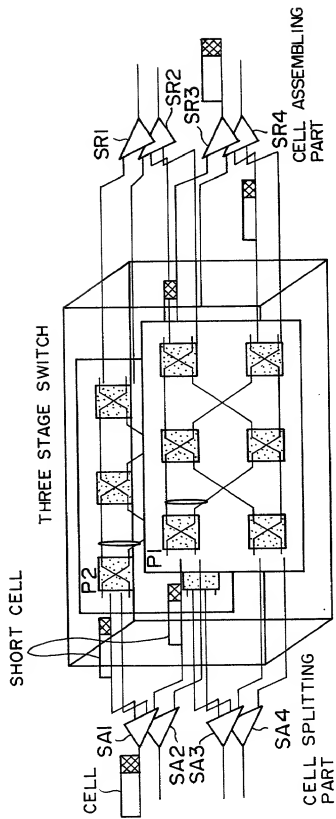
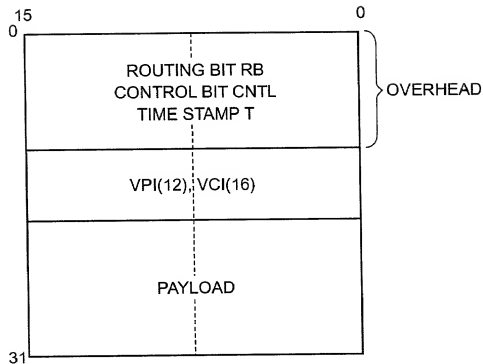


FIG. 24



# FIG.25



# FIG.26

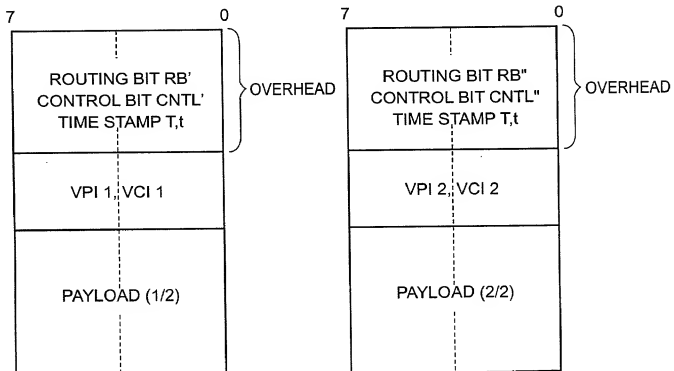


FIG.27

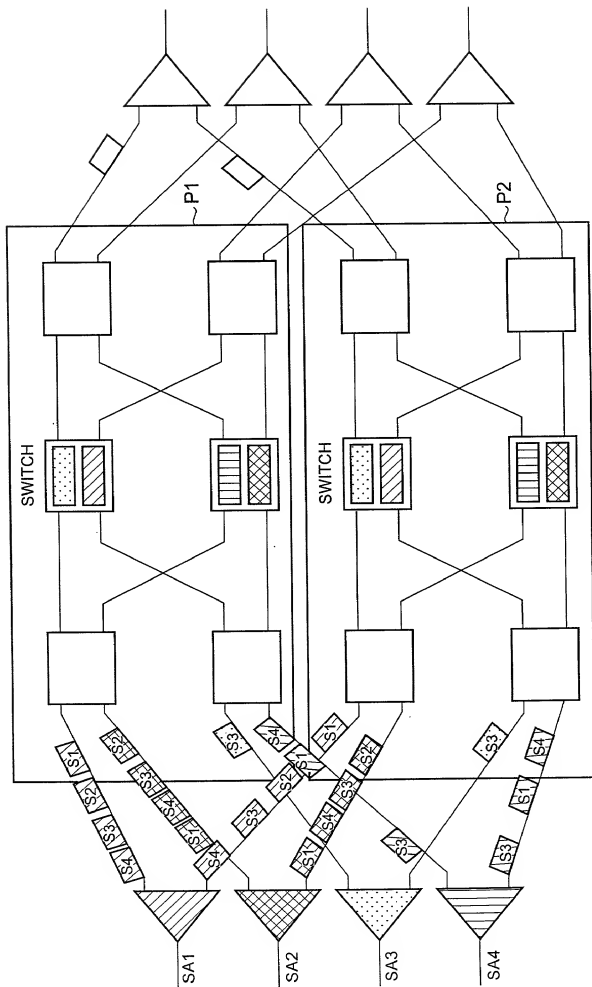


FIG.28

	T1	T2	T3	T4
SA1	S1	S2	S3	S4
SA2	S2	S3	S4	S1
SA3	S3	S4	S1	S2
SA4	S4	S1	S2	S3



FIG.29

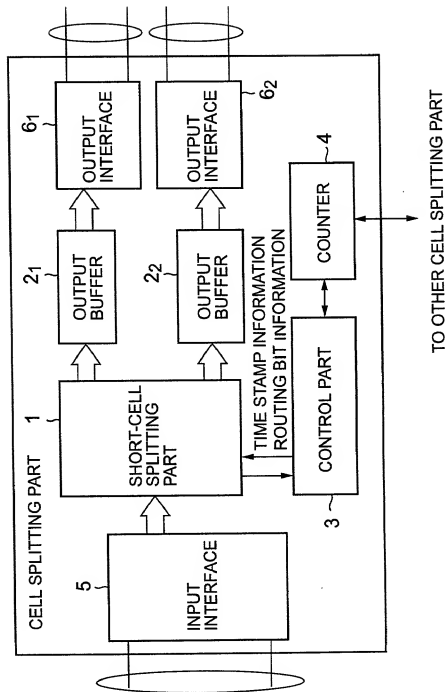


FIG.30

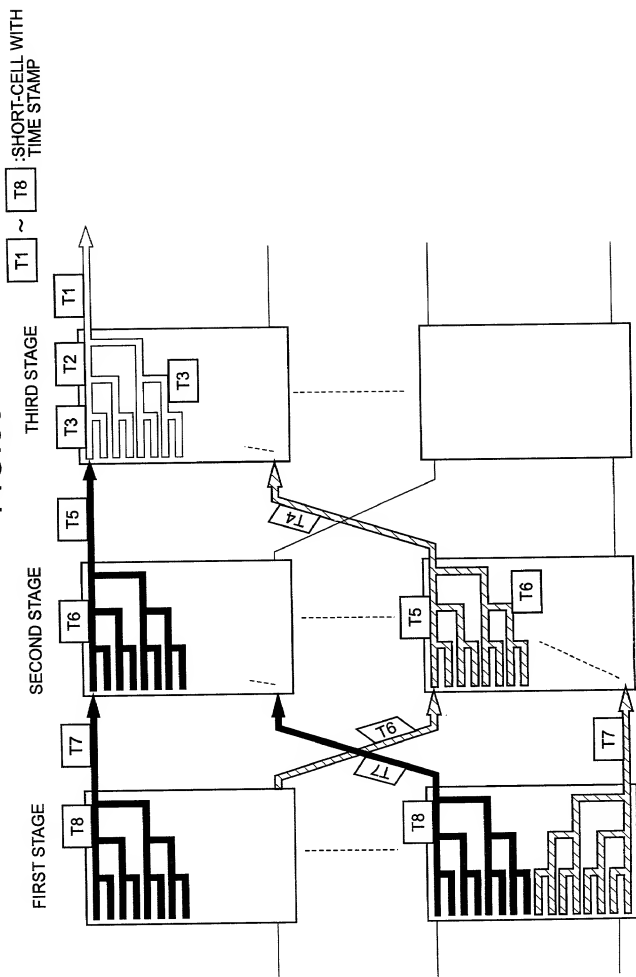


FIG.31

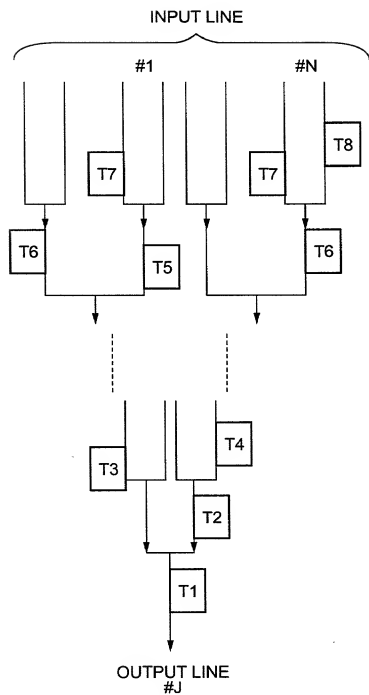




FIG.33

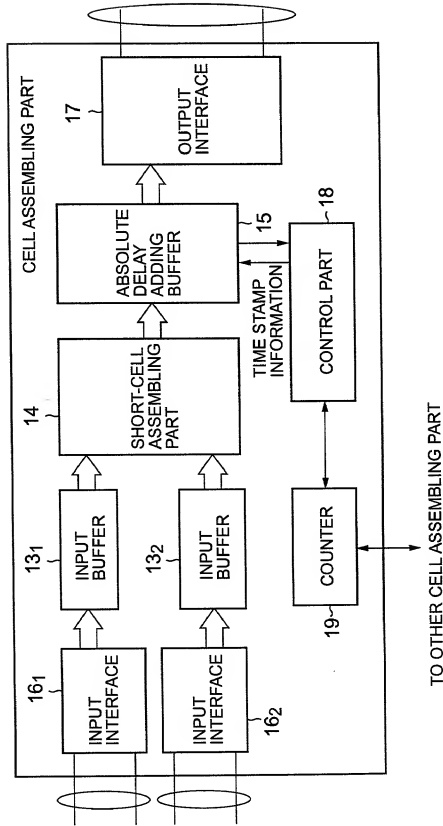


FIG.34

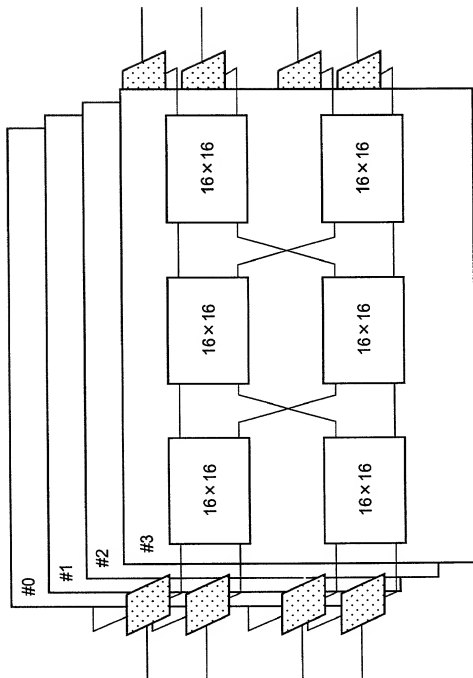


FIG.35

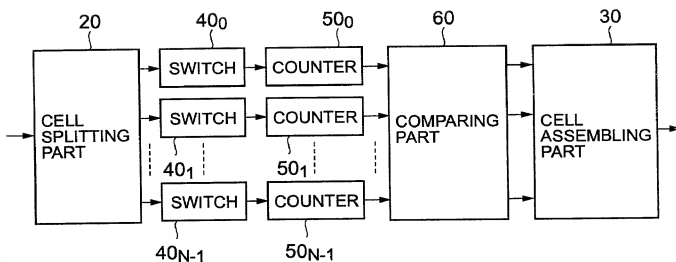


FIG.36

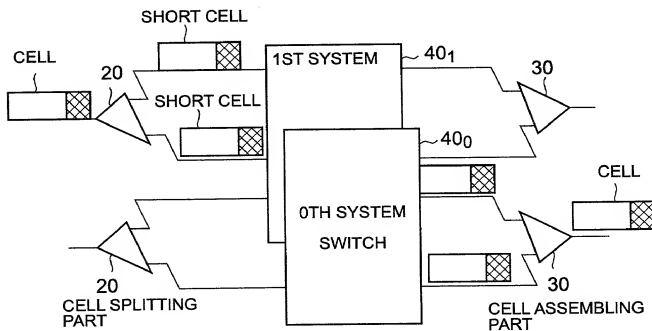


FIG. 37

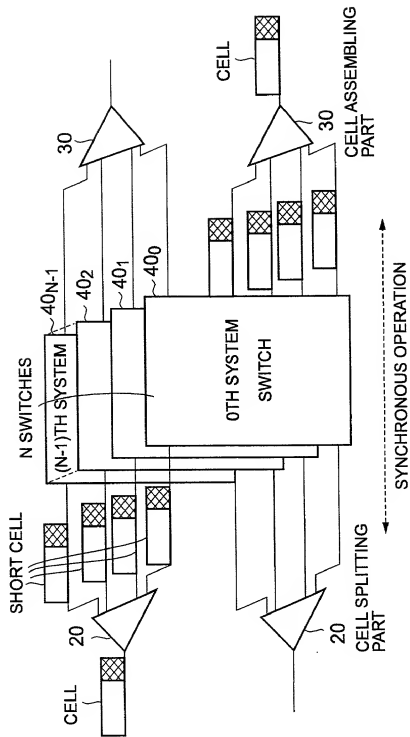




FIG.38

CELL TYPE	PORT NUMBER	DESTINATION BITS	SOURCE BITS	TIME STAMP	ATM CELL (1/2)
--------------	----------------	---------------------	-------------	---------------	----------------

CELL TYPE	PORT NUMBER	DESTINATION BITS	SOURCE BITS	TIME STAMP	ATM CELL (2/2)
--------------	----------------	---------------------	-------------	---------------	----------------

CELL TYPE: 01 EMPTY CELL  
 10 ACTUAL CELL  
 11 TIMING CELL

PORT NUMBER: 00 SYSTEM  
 11 SYSTEM

DESTINATION BITS: FINAL DESTINATION  
 SOURCE BITS: INPUT PORT

FIG. 39

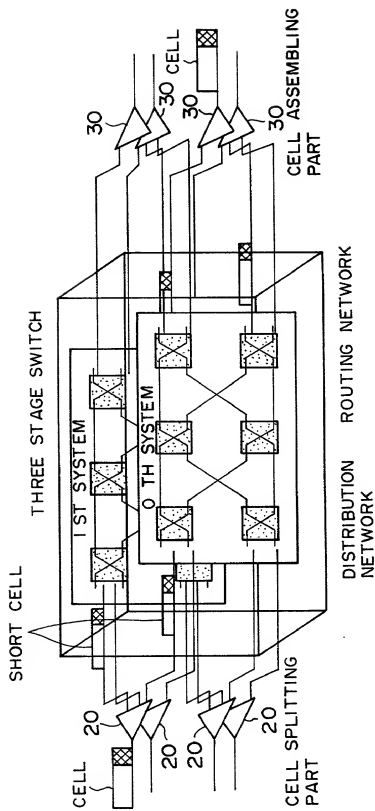


FIG.40

CELL TYPE	PORT NUMBER	DESTINATION BITS	ROUTING BITS	SOURCE BITS	TIME STAMP	ATM CELL (1/2)
--------------	----------------	---------------------	-----------------	----------------	---------------	----------------

CELL TYPE	PORT NUMBER	DESTINATION BITS	ROUTING BITS	SOURCE BITS	TIME STAMP	ATM CELL (2/2)
--------------	----------------	---------------------	-----------------	----------------	---------------	----------------

CELL TYPE: 01 EMPTY CELL  
 10 ACTUAL CELL  
 11 TIMING CELL

PORT NUMBER: 00 SYSTEM  
 11 SYSTEM

ROUTING BITS: DESTINATION SWITCH IN SECOND STAGE  
 DESTINATION BITS: FINAL DESTINATION  
 SOURCE BITS: INPUT PORT

FIG.41

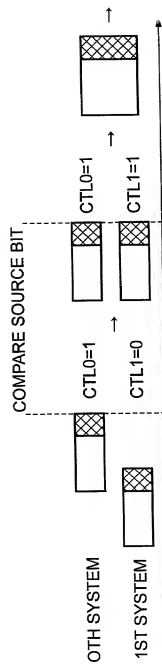
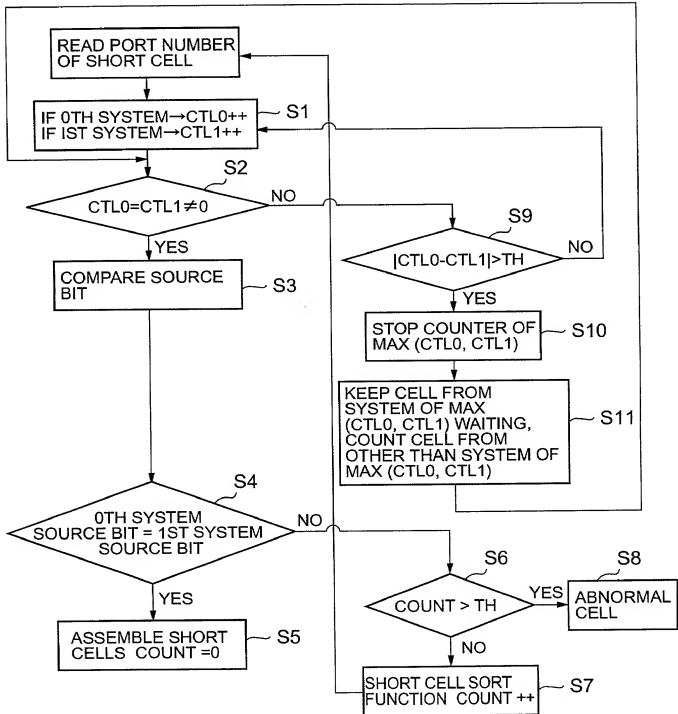


FIG.42



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FIG.43

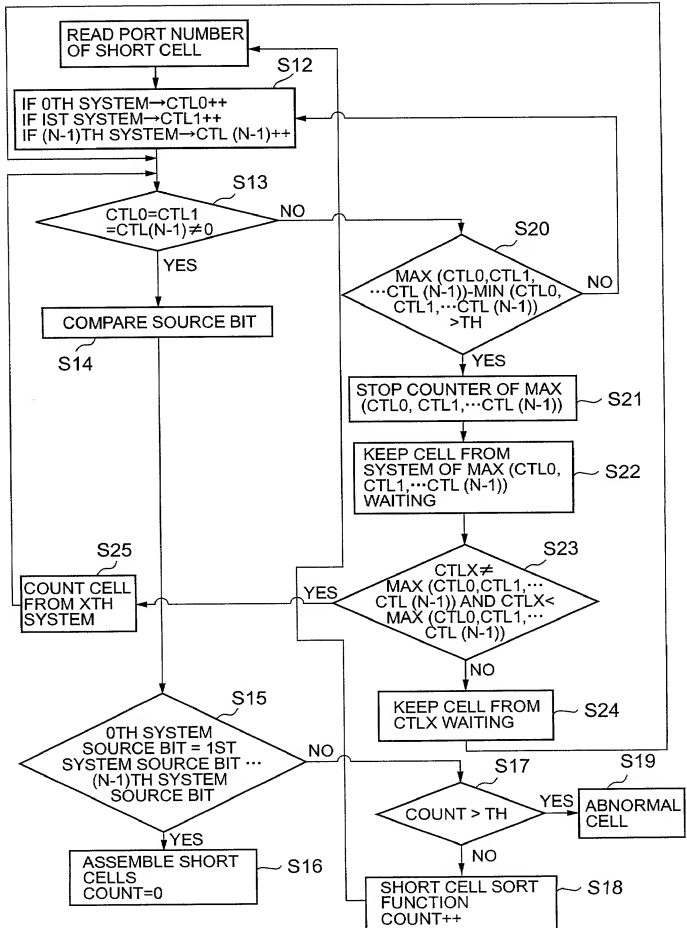


FIG. 44

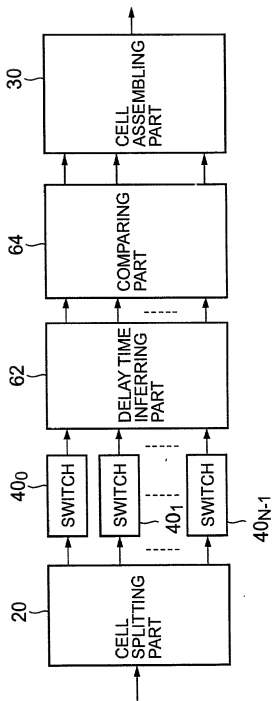


FIG.45

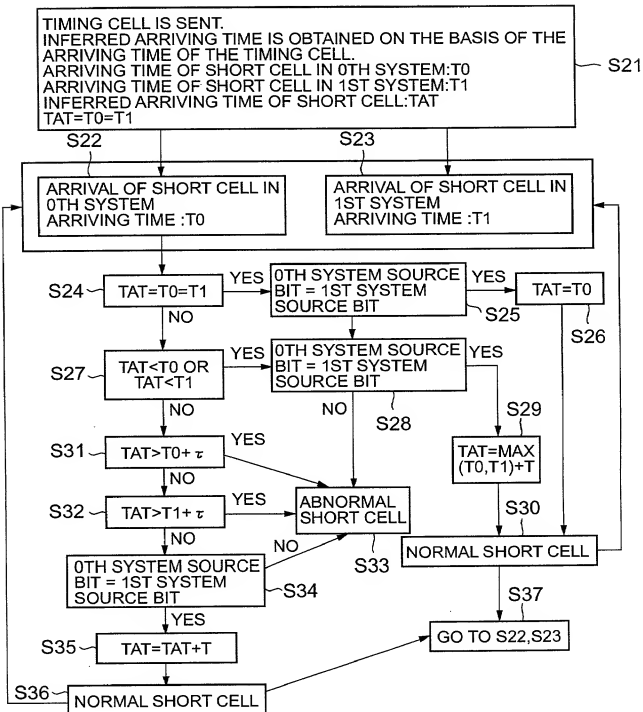




FIG. 46

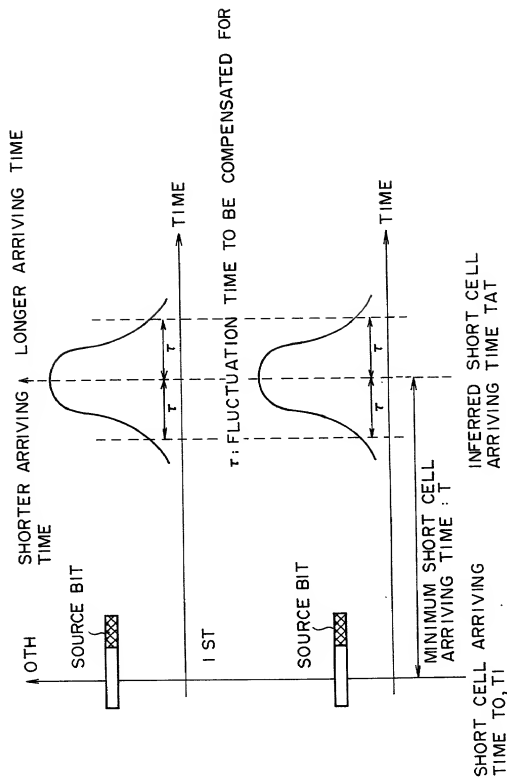


FIG.47A

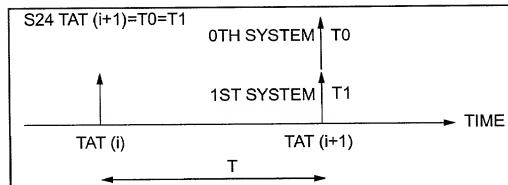


FIG.47B

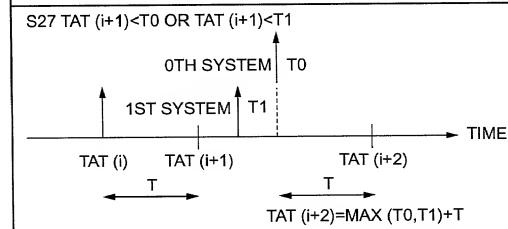


FIG.47C

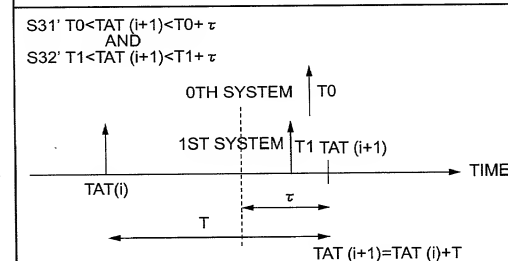


FIG.47D

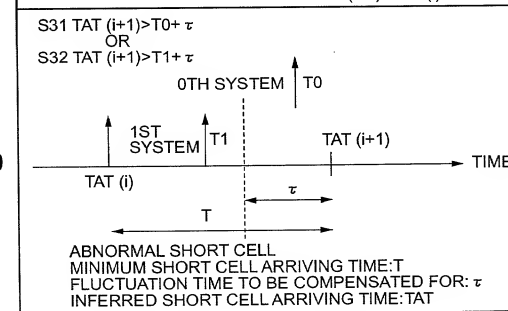
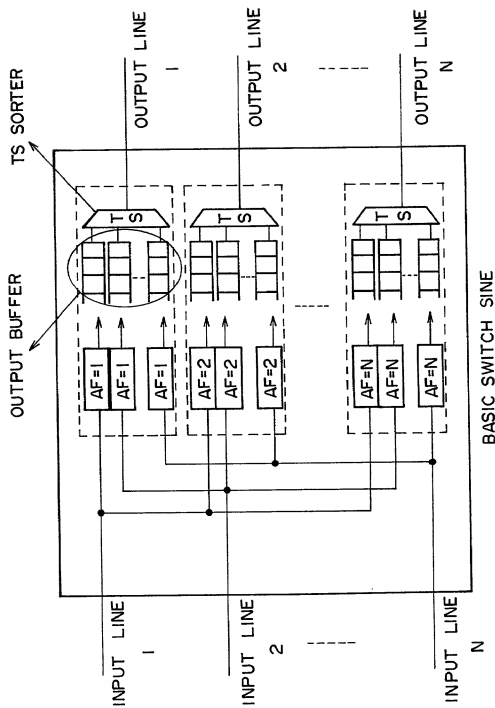
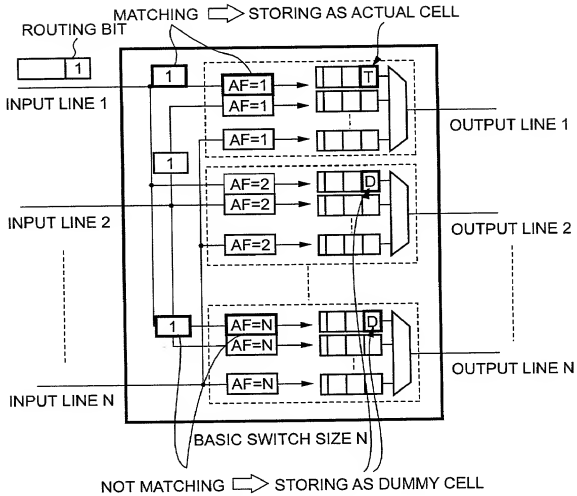


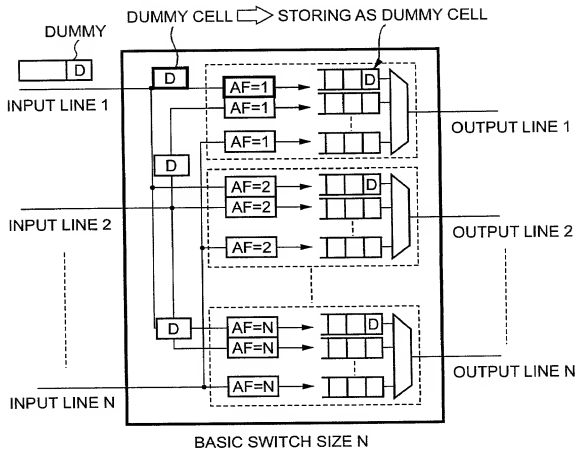
FIG. 48



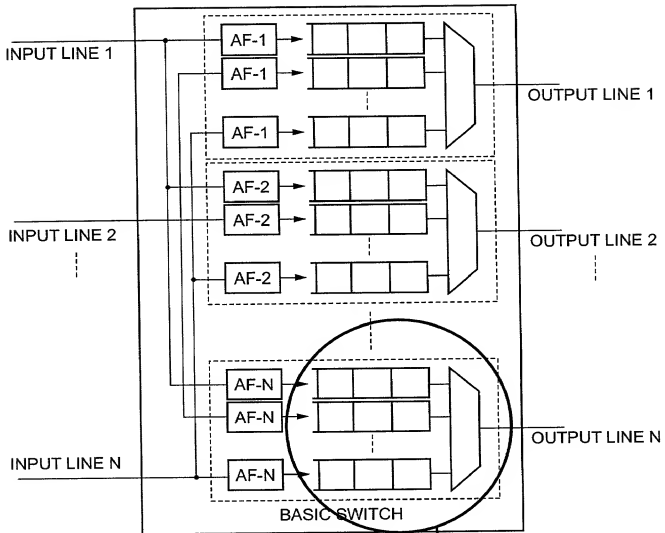
# FIG.49



# FIG.50

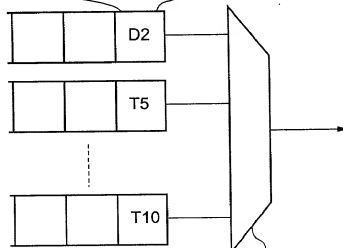


# FIG.51



CELL-TYPE  
(D:DUMMY, T:TRUE)

TIME STAMP (TS)



TIME STAMP-BASED SORTER

FIG.52

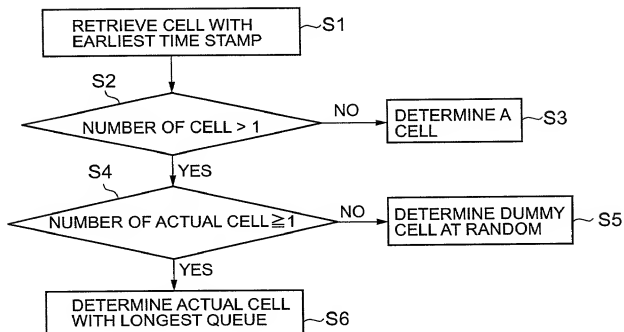


FIG.53

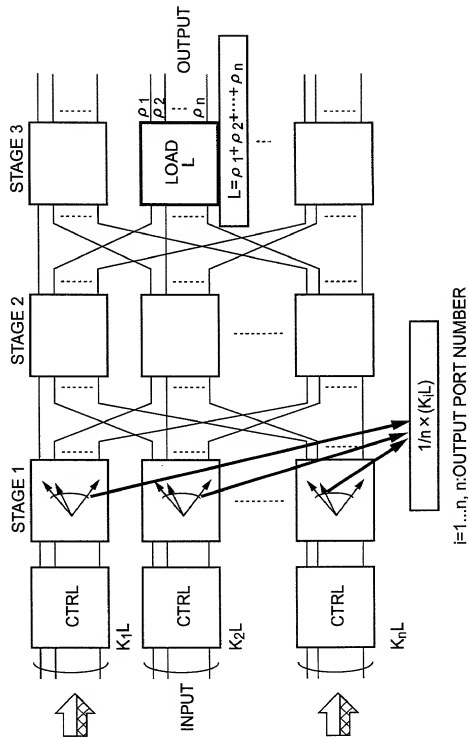




FIG.54

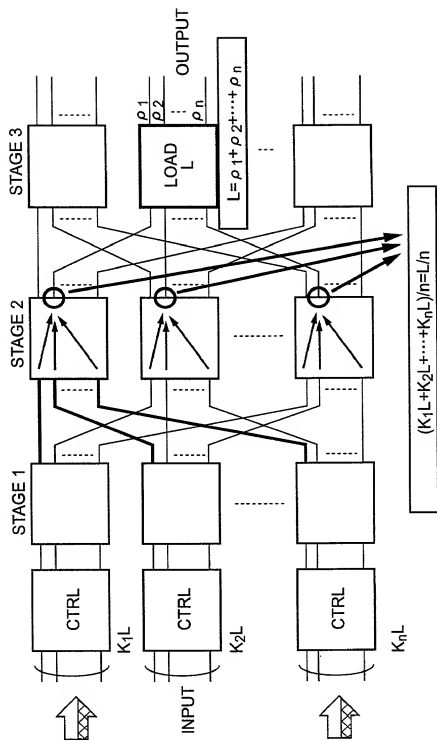


FIG.55

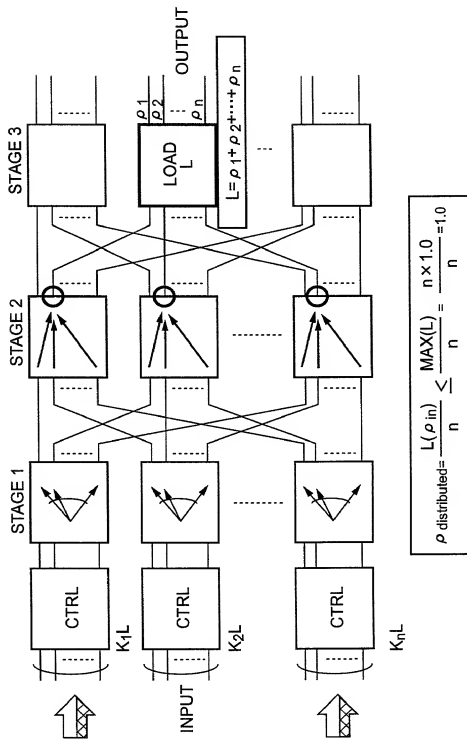


FIG. 56

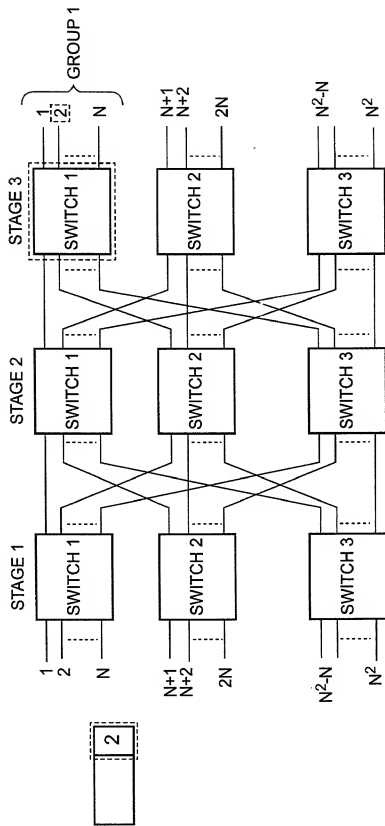


FIG.57

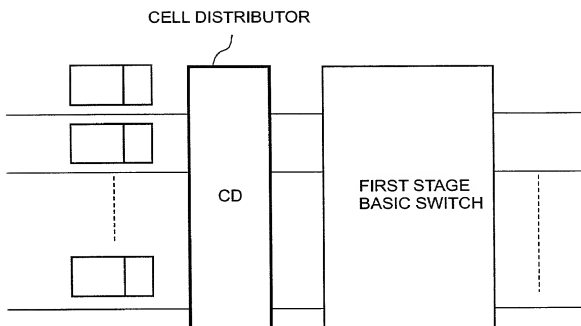


FIG.58

	R1	R2	...	Rn	$\Delta F$
G1	1	0	...	2	2
G2	1	0	...	1	1
:	:	:	...	:	:
Gn			...		

n: SWITCH SIZE

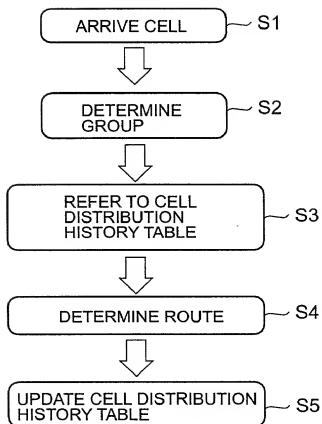


FIG. 60A

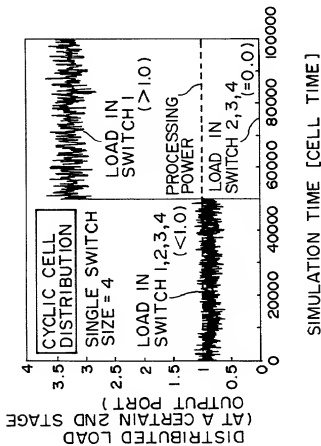


FIG. 60B

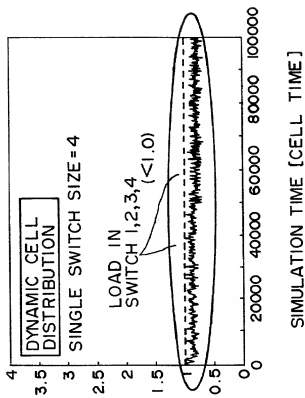


FIG. 61

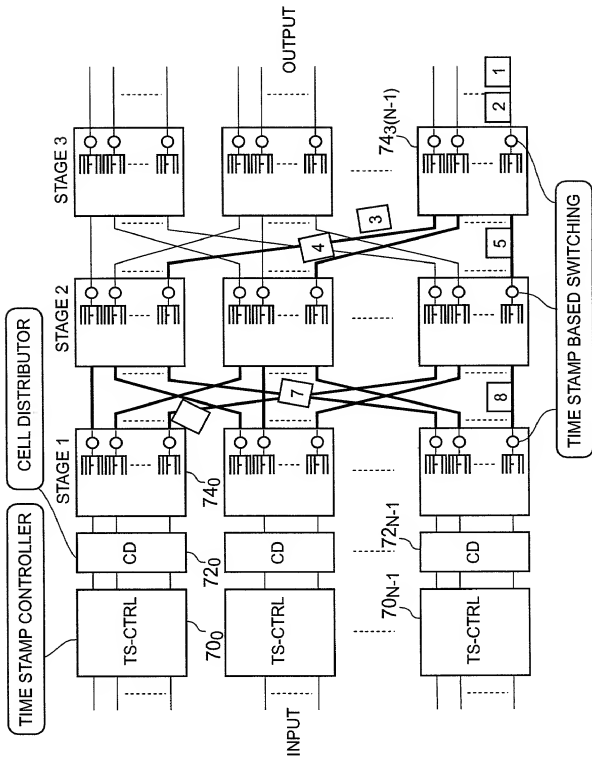




FIG. 62

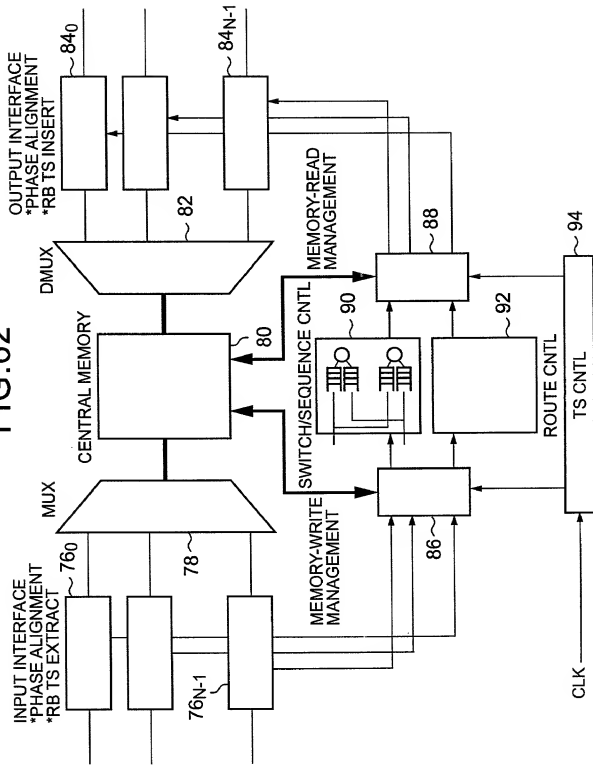


FIG. 63

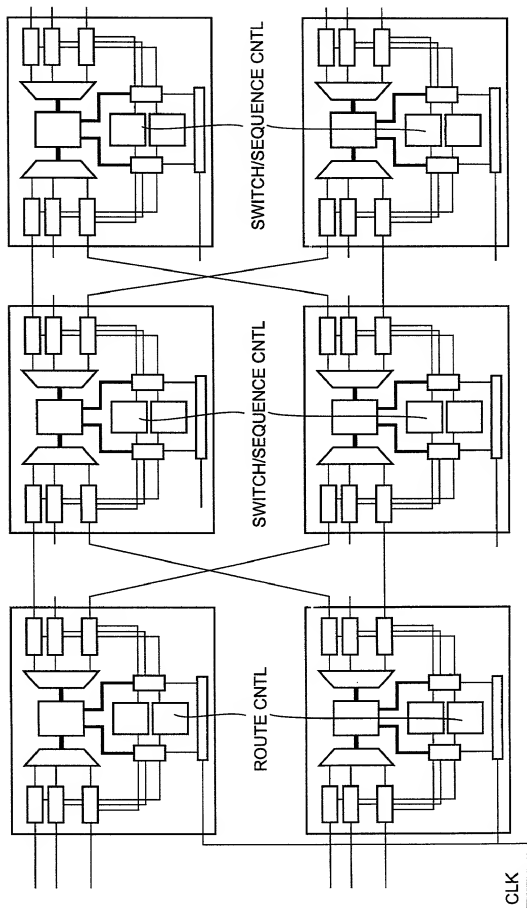


FIG. 64

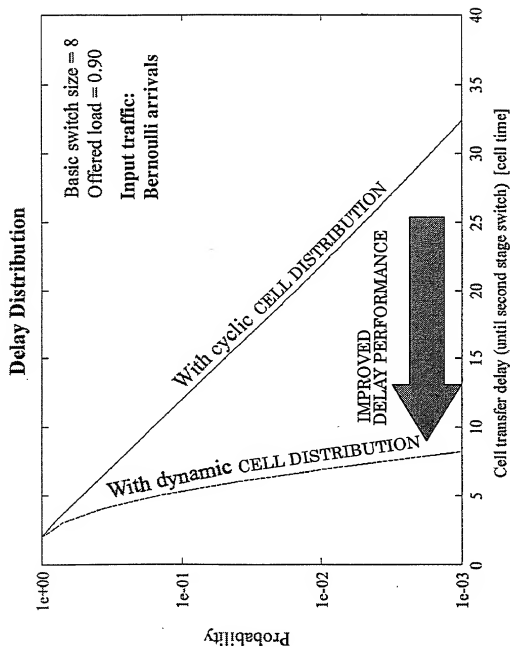


FIG.65

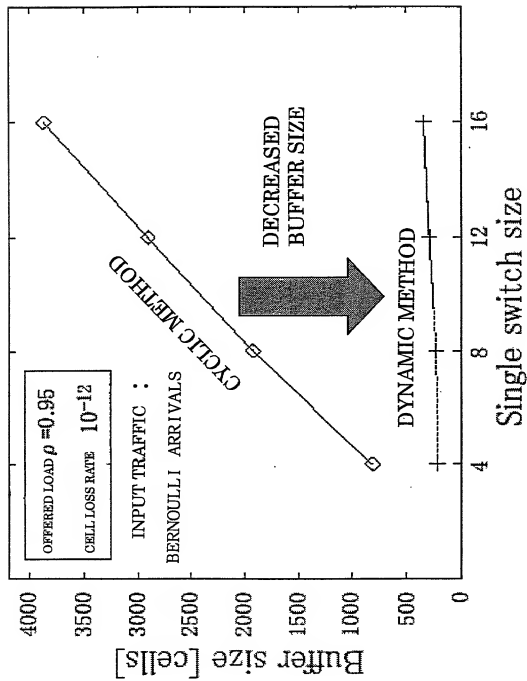
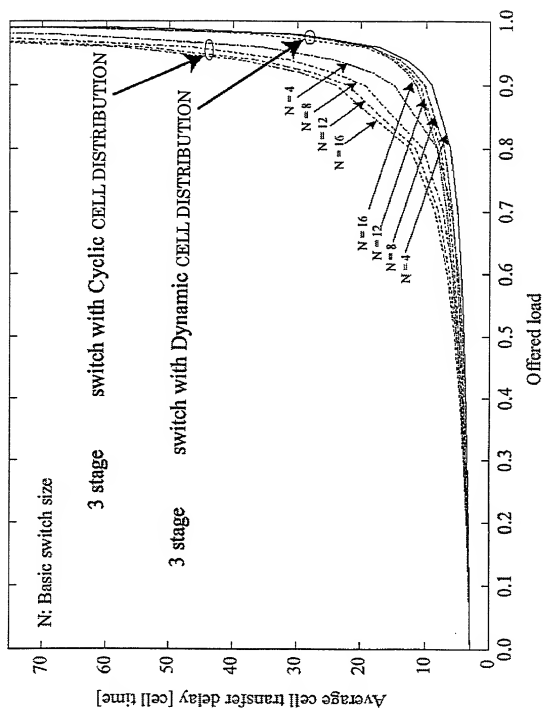
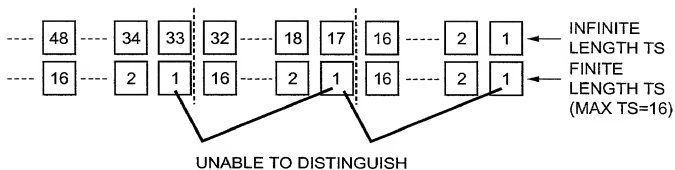


FIG.66

## Cell Transfer Delay Performance



# FIG.67A



# FIG.67B

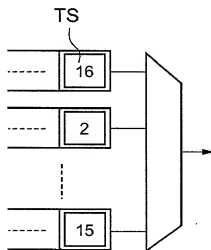


FIG. 68A

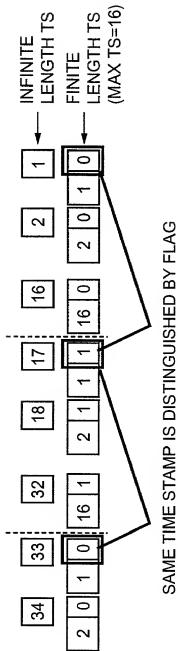
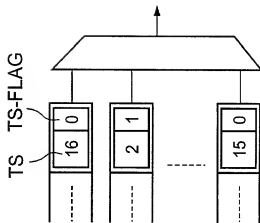
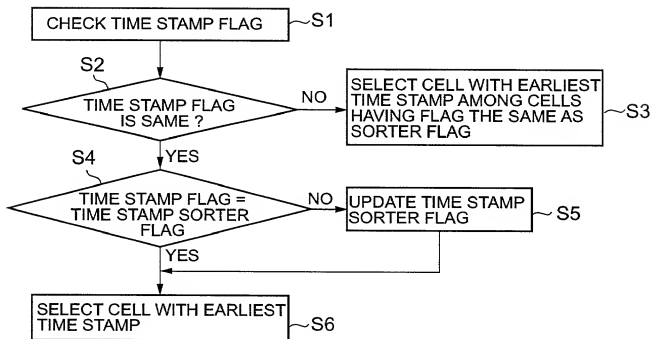


FIG. 68B

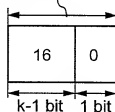


# FIG.69



# FIG.70

TIME STAMP BIT LENGTH =  $k$





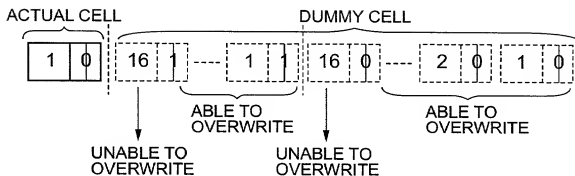
037694 = 037695



FIG.72



# FIG.73



# FIG.74

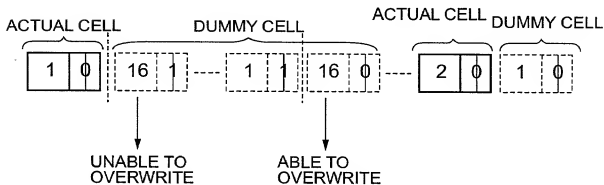


FIG.75

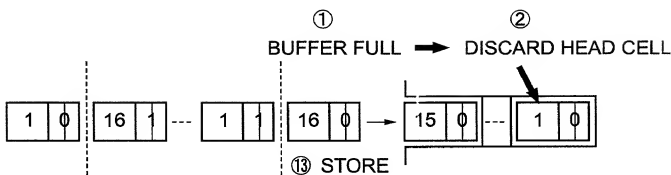


FIG.76

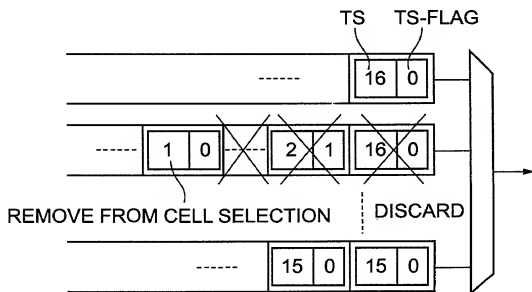


FIG.77

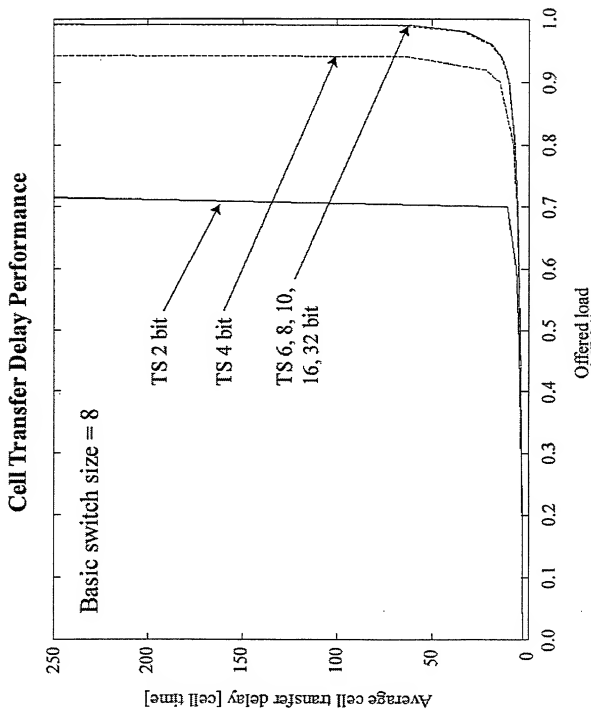


FIG.78

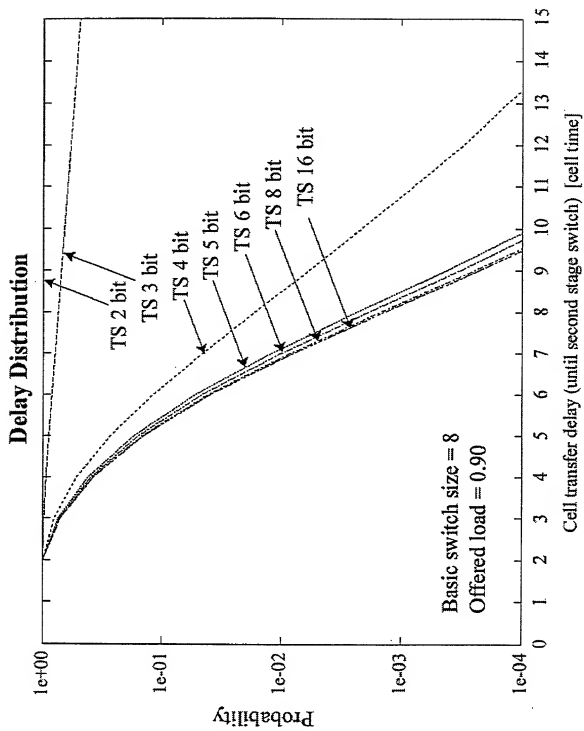


FIG.79

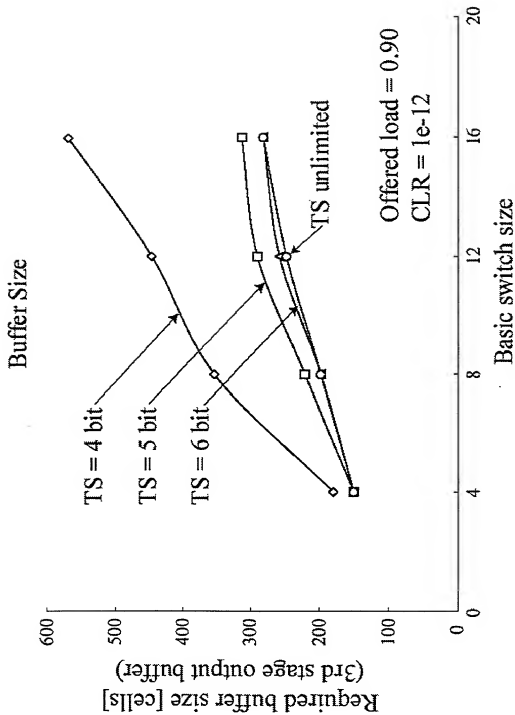


FIG. 80

